CLAIMS

1. A circuit arrangement for transferring data between a data transmitter and a data receiver, said circuit arrangement comprising:

a buffer device that receives a data signal from the data transmitter and provides a buffered data signal onto a data bus;

a first memory element that receives and stores said buffered signal on said data bus and provides a first stored signal;

a second memory element that receives and stores said first stored signal and provides a second stored signal to the data receiver; and

a controller that controls the output state of said buffer device, to control the transfer of data from said first memory element to said second memory element.

2. The circuit arrangement of claim 1, wherein said first memory element comprises by inherent parasitic capacitance associated with said data bus.

3. The circuit arrangement of claim 1, wherein said first memory device is constructed as a capacitive element, one of whose terminals is connected to said data bus , and whose other terminal is connected to a reference potential.

4. The circuit arrangement of claim 3, wherein capacitance of said capacitive element is

provided by the line capacitance of said data bus with respect to one or more reference lines.

5. The circuit arrangement of claim 2, wherein said first memory device comprises a dedicated memory element that comprises a holding element.

6. The circuit arrangement of claim 3, wherein said controller controls said data buffers (P1, P2) associated with the data transmitter (S) and the data receivers (E), and the second memory devices (Sp2).

7. The circuit arrangement of claim 1, wherein said controller comprises:

a first control section, associated with the data transmitter, for controlling the first data buffer; and

a second control section, associated with each of the data receivers, that controls second data buffers and said second memory devices, a control data communication between the data transmitter and the data receiver.

8. The circuit arrangement of claim 7, wherein at least one of the circuit sections (1, 2) is part of a peripheral region (2) of the integrated circuit for accepting the connection pads of the input/output connections.

9. The circuit arrangement of claim 1, wherein the circuit arrangement has at least one

microprocessor/microcontroller and/or at least one signal processor with a given set of states.

10. The circuit arrangement of claim 1, wherein said first memory element consists of parasitic capacitance associated with said data bus.

11. An integrated circuit arrangement for transferring data between a data transmitter and a data receiver, said circuit arrangement comprising:

means for receiving a data signal from the data transmitter and for providing a buffered data signal onto a data bus;

a first memory element that receives and stores said buffered signal on said data bus, and provides a first stored signal;

a second memory element that receives and stores said first stored signal, and provides a second stored signal to the data receiver; and

a controller that controls the output state of said means for receiving, such that when said means for receiving provides a high impedance output data is transferred from said first memory element to said second memory element.